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National Semiconductor®

Geode™ CS4103
IEEE P1394a Physical Layer Device

General Description

The National Semiconductor® Geode™ CS4103 is a three port 400 Mbit/sec IEEE 1394 Physical Layer (PHY) device. The CS4103 complies to revision 2.0 of the P1394a specification. The device is a three port implementation of a reusable cell design scalable from one to sixteen ports.

The CS4103 supports all of the P1394a enhancements including connection debounce, arbitrated reset, ack-accelerated arbitration, fly-by concatenation, multi-speed packet concatenation, PHY pinging, priority arbitration, and Suspend/Resume operation. It also implements the standard PHY-Link interface defined in IEEE specification 1394-1995 and updated in the P1394a specification for direct connection with the Geode CS4210 IEEE 1394 Open Host Controller Interface (OHCI) device. The interface can operate in either direct or isolated mode and supports single capacitor isolation with bus hold inputs.

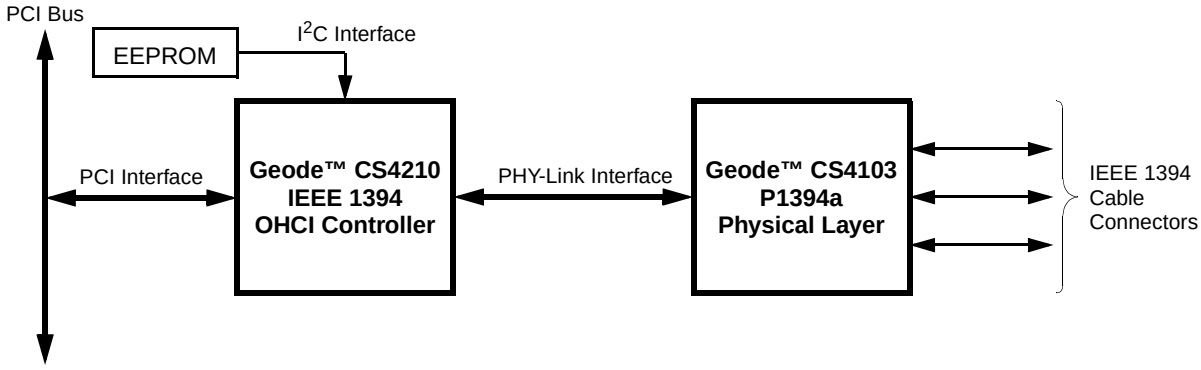
The CS4103 provides a complete PHY solution including all bias generation, differential line drivers and receivers, single ended comparators for speed signaling, speed signaling current sources, bias detect, and connect detect circuitry per port. It includes data and strobe encoding/decoding functions as well as a re-time FIFO to synchronize the receive data to the local clock domain. The CS4103 can receive and respond to all the PHY packet types defined in revision 2.0 of the P1394a specification. It also supports Suspend and Resume port states and connect detect functions.

The CS4103 generates the internal clocks and the Link SCLK (System Clock) based on a 24.576 MHz external crystal or a 24.576 MHz clock input. The CS4103 operates from a single 3.3V supply and supports transfers at 98.304, 196.608, and 393.216 Mbit/sec, (usually referred to as 100, 200, and 400 Mbit/sec respectively).

Features

- IEEE 1394 Physical Layer Device (PHY) compliant with revision 2.0 of P1394a including all enhancements
- Scalable design from one to sixteen ports
- Supports data rates of 100, 200, and 400 Mbit/sec
- Single 3.3V supply operation
- Internal PLL generates SCLK and all internal clocks from a single 24.576 MHz crystal or clock
- Includes Cable Power Sense comparator for cable power monitoring
- Compatible with the Geode CS4210 OHCI Controller and other IEEE 1394 OHCI devices
- Supports the isolated PHY-Link interface compliant with 1394-1995 and P1394a specifications
- Single capacitor bus hold isolation\
- Power saving modes
- 80-pin TQFP (Thin Quad Flat Pack)

System Block Diagram



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1.0 Architectural Overview

The Geode CS4301 can be described as providing the functional blocks as shown in Figure 1-1 and described in the following subsections.

1.1 LINK INTERFACE

The Link Interface implements the PHY-Link Interface as specified in clause 5, revision 2.0 of the P1394a specification. It handles both differentiated and undifferentiated modes of operation. It decodes LREQ requests and communicates with the Arbiter and Register Set for bus requests and register read/write commands, respectively. In addition to receiving LREQ requests, the Link Interface handles the bidirectional control and data buses for packet transmission and reception as well as register reads. The Link Interface uses the Link Power Status input (LPS) signal to determine the operational state of the Geode CS4210 OHCI Controller and for resetting, disabling, and/or restoring the PHY-Link Interface. The Link Interface also controls the Link-On output (LNKON), used to signal the CS4210 when the PHY-Link Interface is not active.

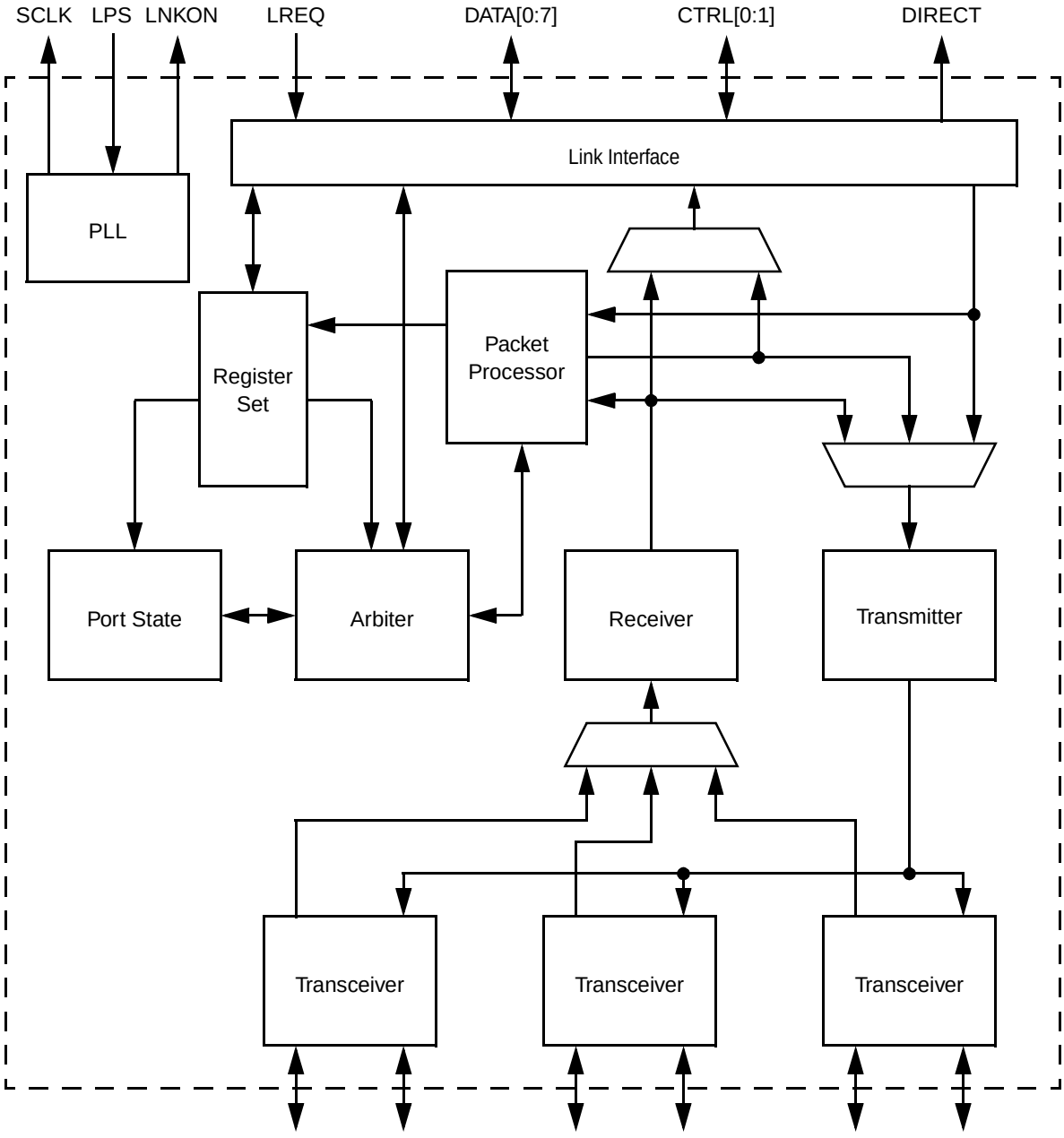


Figure 1-1. Functional Block Diagram

Architectural Overview (Continued)

1.2 ARBITER

The Arbiter includes the logic to implement all of the state machines described in clause 7, revision 2.0 of the P1394a specification except for the Port State machine. These include the state machines for bus reset, Tree-ID, Self-ID, and normal arbitration. The Arbiter monitors the received line states and controls the transmitted and repeated line states for the various types of arbitration processes. The Arbiter maintains the arbitration timer responsible for timing the various gaps and line state lengths required for P1394a operation. It also receives bus requests from the CS4210 via the Link Interface and sends the appropriate handshake signals to indicate won/lost status to the Link Interface.

1.3 REGISTER SET

The Register Set implements all of the registers defined in the P1394a specification. The Register Set has interfaces to the Link Interface module for register reads and writes as well as to the Packet Processor for register reads. The Register Set also contains several National Semiconductor specific register bits implemented in the address page which are set aside for vendor specific registers and interfaces with the Arbiter and Port State. For example, the Root hold-off bit affects the Arbiter and the Port Disabled bits affect the operation of the Port State.

1.4 PACKET PROCESSOR

The Packet Processor decodes all PHY packets received by the CS4103, (from both the CS4210 and cable interfaces) and generates all PHY response packets that the CS4103 must send autonomously. The Packet Processor also provides validity checking on PHY packets, discarding invalid packets. During bus initialization and configuration, the Packet Processor signals the reception of Self-ID packets to the Arbiter. The Arbiter uses this information during the Self-ID process to increment the Node ID count.

1.5 PORT STATE

The Port State contains the Port Connection State Machine described in clause 7.10.4, revision 2.0 of the P1394a specification. The Port State keeps track of the connect status and state of each port, (Disconnect, Resuming, Active, etc.). The Port State also implements the connection timer used for timing various transitions within the state machine and reports certain state conditions to other modules. For example, the Port State signals the Arbiter with the Active, Resume, and Suspend state of each port along with other status information. It also reports connection change information for waking the CS4103 from a low-power mode.

1.6 RECEIVER

The Receiver consists of the logic responsible for the data/strobe decoding, the serial-to-parallel converter, and the re-time FIFO. During packet reception and repeating, the re-time FIFO buffers the data to allow for frequency differences between the transmitting and receiving PHYs. The CS4103 writes data into the FIFO using the recovered clock from the incoming data stream. It removes data from the FIFO using the local system clock. The size of the FIFO is calculated to allow the successful reception of a maximum length packet with a maximum clock offset between this PHY and the Transmitter.

1.7 TRANSMITTER

The Transmitter handles the parallel-to-serial conversion and data/strobe encoding operations. It can transmit data from one of three sources: the Link Interface, the on-chip Packet Processor, and the repeat path. The Arbiter controls which path is selected for each transmit operation.

1.8 TRANSCEIVER

The Transceiver handles the interface to the 1394 cable. It has drivers and receivers for the cable wires, (TPA+, TPA–, TPB+, and TPB–). In addition, each Transceiver provides a TpBias output for its port. On transmit, the Transceiver generates the appropriate speed signaling for 100, 200, and 400 Mbit/sec operation. The Transceiver also transmits 1, 0, and Z values on each differential pair (TPA and TPB). The Receiver detects speed signaling values and the Arbitration line states (1, 0, and Z). It contains separate differential receivers used to interpret data and strobe during packet reception.

The Transceiver logic contains TpBias detection circuitry as well as a Connect Detect circuit. The Transceiver enables the Connect Detect circuit when the Port State logic instructs the Transceiver to turn off the TpBias generation, (for example, when the port enters the Suspend state).

1.9 PHASE-LOCKED LOOP (PLL)

The PLL module uses a 24.576 MHz crystal or clock input to generate all of the local clocks. These include the 49.152 MHz system clock (SCLK) as well as the 98.304 MHz, 196.698 MHz, and 393.216 MHz clocks necessary for transmitting at 100, 200, and 400 Mbit/sec. This PLL design requires no external filter components.

1.10 RELATED DOCUMENTS

The following documents may be useful in understanding the terms and concepts used in this publication.

- IEEE Standard 1394-1995 “IEEE Standard for a high performance serial Bus”
- P1394a Draft 2.0 “P1394a Draft Standard for a High Performance Serial Bus” (supplement)

2.0 Signal Definitions

This section defines the signals and external interface of the CS4103. Figure 2-1 shows the pins organized by their functional groupings (internal test and electrical pins are not shown).

2.1 PIN ASSIGNMENT

The tables in this section use several common abbreviations. Table 2-1 lists the mnemonics and their meanings.

Figure 2-2 on page 6 shows the pin assignment for the CS4103 with Tables 2-2 and 2-3, on pages 7 and 8, listing the pin assignments sorted by pin number and alphabetically by signal name.

Section 2.2 "Signal Descriptions" starting on page 9 provides a description for each signal within its associated functional group.

Table 2-1. Pin Type Definitions

Mnemonic	Definition
I	Input Pin
I/O	Bidirectional Pin
O	Output
t/s	TRI-STATE Signal
VDD	2.5V Core Power Supply
VDDIO	3.3V I/O Power Supply
VSS	Ground Connection

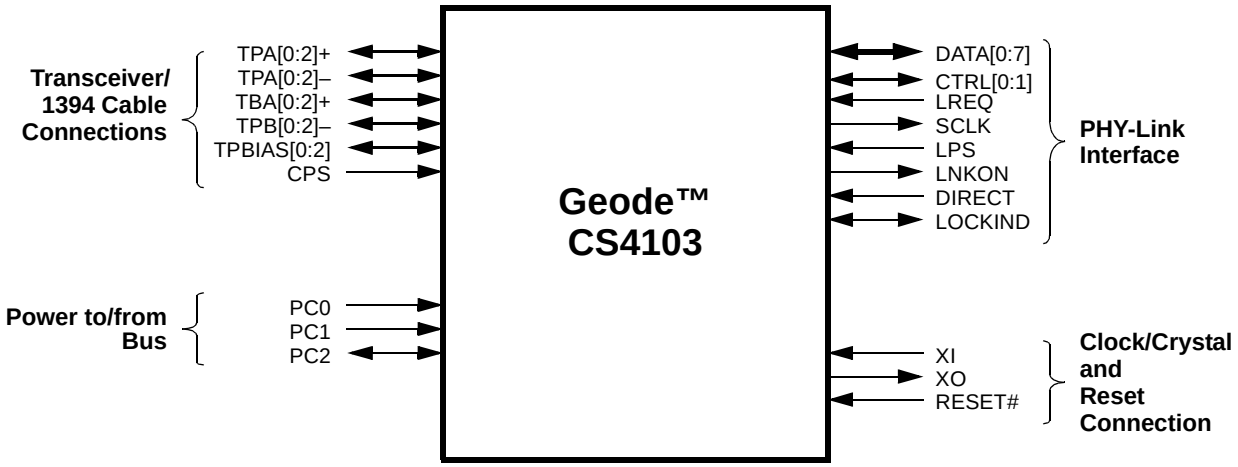


Figure 2-1. Signal Groups

Signal Definitions (Continued)

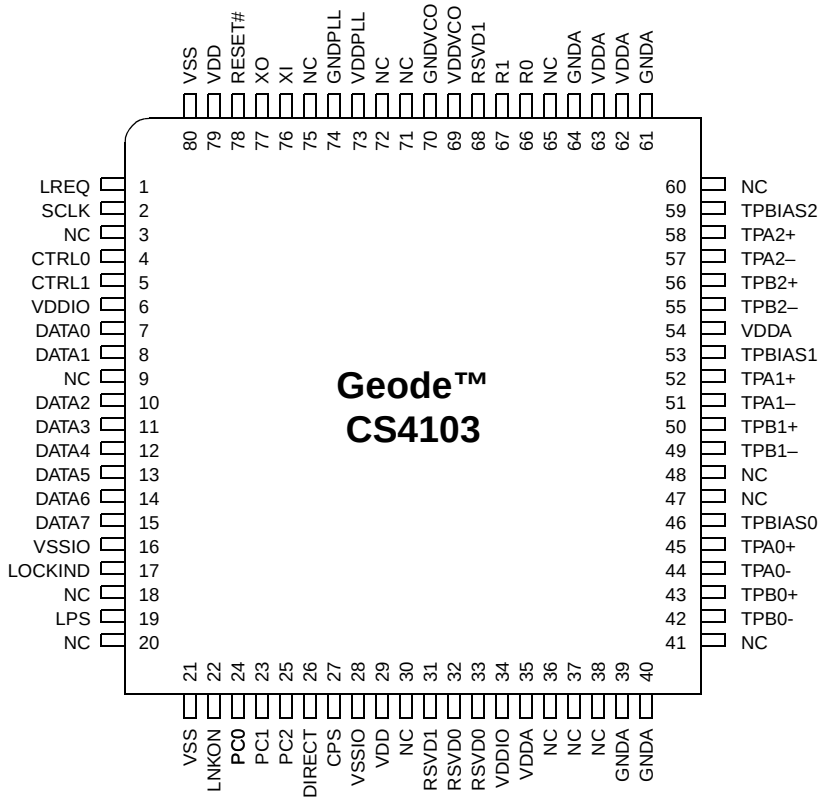


Figure 2-2. Pin Assignment Diagram
Order number: CS4103VHG

Signal Definitions (Continued)

Table 2-2. Pin Assignment - Sorted by Pin Number

Pin No.	Signal	Type
1	LREQ	I
2	SCLK	O
3	NC	--
4	CTRL0	I/O
5	CTRL1	I/O
6	VDDIO	PWR
7	DATA0	I/O
8	DATA1	I/O
9	NC	--
10	DATA2	I/O
11	DATA3	I/O
12	DATA4	I/O
13	DATA5	I/O
14	DATA6	I/O
15	DATA7	I/O
16	VSSIO	PWR
17	LOCKIND	I/O
18	RSVD NC	--
19	LPS	I
20	NC	--
21	VSS	GND
22	LNKON	O
23	PC0	I
24	PC1	I
25	PC2	I/O
26	DIRECT	I
27	CPS	I
28	VSSIO	GND
29	VDD	PWR
30	NC	--
31	RSVD1	I
32	RSVD0	I
33	RSVD0	I
34	VDDIO	I/O
35	VDDA	PWR
36	NC	--
37	NC	--
38	NC	--
39	GNDA	GND
40	GNDA	GND
41	NC	--
42	TPB0–	I/O
43	TPB0+	I/O
44	TPA0–	I/O
45	TPA0+	I/O
46	TPBIAS0	I/O
47	NC	--
48	NC	--
49	TPB1–	I/O
50	TPB1+	I/O
51	TPA1–	I/O
52	TPA1+	I/O
53	TPBIAS1	I/O
54	VDDA	PWR
55	TPB2–	I/O
56	TPB2+	I/O
57	TPA2–	I/O
58	TPA2+	I/O
59	TPBIAS2	I/O
60	NC	--
61	GNDA	GND
62	VDDA	PWR
63	VDDA	PWR
64	GNDA	GND
65	NC	--
66	R0	--
67	R1	--
68	RSVD1	I
69	VDDVCO	PWR
70	GNDVCO	GND
71	NC	--
72	NC	--
73	VDDPLL	PWR
74	GNDPLL	GND
75	NC	--
76	XI	I
77	XO	O
78	RESET#	I
79	VDD	PWR
80	VSS	GND

Signal Definitions (Continued)

Table 2-3. Pin Assignment - Sorted Alphabetically

Signal	Type	Pin No.
CPS	I	27
CTRL0	I/O	4
CTRL1	I/O	5
DATA0	I/O	7
DATA1	I/O	8
DATA2	I/O	10
DATA3	I/O	11
DATA4	I/O	12
DATA5	I/O	13
DATA6	I/O	14
DATA7	I/O	15
DIRECT	I	26
GNDA	GND	39
GNDA	GND	40
GNDA	GND	61
GNDA	GND	64
GNDPLL	GND	74
GNDVCO	GND	70
LNKON	O	22
LOCKIND	I/O	17
LPS	I	19
LREQ	I	1
NC	--	3
NC	--	9
NC	--	20
NC	--	30
NC	--	36
NC	--	37
NC	--	38
NC	--	41
NC	--	47
NC	--	48
NC	--	60
NC	--	65
NC	--	71
NC	--	72
NC	--	75
NC	--	18
PC0	I	23
PC1	I	24
PC2	I/O	25
R0	--	66
R1	--	67
RESET#	I	78
RSVD0	I	32
RSVD0	I	33
RSVD1	I	31
RSVD1	I	68
SCLK	O	2
TPA0–	I/O	44
TPA0+	I/O	45
TPA1–	I/O	51
TPA1+	I/O	52
TPA2–	I/O	57
TPA2+	I/O	58
TPB0–	I/O	42
TPB0+	I/O	43
TPB1–	I/O	49
TPB1+	I/O	50
TPB2–	I/O	55
TPB2+	I/O	56
TPBIAS0	I/O	46
TPBIAS1	I/O	53
TPBIAS2	I/O	59
VDD	PWR	29
VDD	PWR	79
VDDA	PWR	35
VDDA	PWR	54
VDDA	PWR	62
VDDA	PWR	63
VDDIO	PWR	6
VDDIO	I/O	34
VDDPLL	PWR	73
VDDVCO	PWR	69
VSS	GND	21
VSS	GND	80
VSSIO	PWR	16
VSSIO	GND	28
XI	I	76
XO	O	77

Signal Definitions (Continued)

2.2 SIGNAL DESCRIPTIONS

2.2.1 PHY-Link Interface Signals

Signal Name	Pin	Type	Description
CTRL[0:1]	4, 5	I/O	**Control Bits 0 and 1** The CS4103 uses CTRL[0:1] to signal PHY status transfers and packet reception transfers to the CS4210. The CS4103 grants control of the interface to the CS4210 for packet transmission.
DATA[0:7]	7, 8, 10:15	I/O	**Data Bits 0 through 7** DATA[0:1] are used for PHY status data transfers to the CS4210 and packet transmit and receive. The width of the data bus depends on the speed of data transfer rate. Packet rate for 100 Mbit/sec transfers use DATA[0:1], 200 Mbit/sec transfers use DATA[0:3], 400 Mbit/sec transfers use DATA[0:7]. **Note:** DATA0 is considered the MSB (most significant bit) based upon the IEEE 1394-1995 specification.
LREQ	1	I	**Link Request** The CS4103 receives serial bit stream requests from the CS4210 on this line. The requests write PHY registers, request PHY register data, request packet transmission, and control arbitration acceleration.
SCLK	2	O	**System Clock** The 49.152 MHz clock output driven by the CS4103's PLL block synchronized to the 1394 bus clock. This clock is also used to synchronize the LREQ, CTRL[0:1], and DATA[0:7] communication protocol between the CS4210 and CS4103.
LPS	19	I	**Link Power Status** The CS4210 signals the CS4103 to both reset and disable the PHY-Link interface when this input is deaserted and to restore the interface when asserted. This line is level driven in direct mode and pulsed in isolated mode.
LNKON	22	O	**Link-On** The CS4103 uses this output to signal the CS4210 when the Link is inactive. The Link is inactive when either LPS is deaserted or the PHY-Link_active bit (Address 04h[0]) is zero. LNKON is a pulsed signal with a frequency from 4 to 8 MHz.
DIRECT	26	I	**Direct/Isolation Barrier Indicator** Configures the PHY-Link interface to operate in direct/single capacitor bus hold mode when high or isolated mode when low.
LOCKIND	17	I/O	**PLL Lock Indicator** An output high on this pin indicates that the PLL is locked. This signal is informational and is not required for operation. For normal operation, this pin may be disconnected.

Signal Definitions (Continued)

2.2.2 Transceiver/1394 Cable Connection Signals

Signal Name	Pin	Type	Description
TPB[0:2]–	42, 49, 55	I/O	**Negative Differential Signals for Port 0-2 Cable Pair B** Differential signal skew should be minimized by matching trace lengths within the TPA and TPB differential pairs. In addition, TPA pair trace lengths should be matched as closely as possible to TPB pair trace lengths within a port. Impedance discontinuities may be minimized by routing TP lines primarily on the top layer of the PCB. TP signal traces should have an impedance of 55 ohms to analog ground and the analog ground plane should be continuous under the TP traces. Minimize stub length by placing termination networks as close to the CS4103 as possible.
TPB[0:2]+	43, 50, 56	I/O	**Positive Differential Signals for Port 0-2 Cable Pair B** Refer to TPB[0:2]– signal description.
TPA[0:2]–	44, 51, 57	I/O	**Negative Differential Signals for Port 0-2 Cable Pair A** Refer to TPB[0:2]– signal description.
TPA[0:2]+	45, 52, 58	I/O	**Positive Differential Signals for Port 0-2 Cable Pair A** Refer to TPB[0:2]– signal description.
TPBIAS[0:2]	46, 53, 59	I/O	**Twisted Pair Bias for Port 0-2** Bias generator output and connection detect input for the ports. Increase the PCB trace widths on this line.
CPS	27	I	**Cable Power Status Input** This comparator input detects valid cable power at voltages greater than 7.5V and sets the PS (cable power active) bit (Address 00h[7]) in the CS4103 base register. Voltages below 7.5V clear the PS bit. This pin is connected to a 402K 1% resistor to cable power and an 80.6K 1% resistor to ground.

2.2.3 Clock/Crystal Connection and Reset Signals

Signal Name	Pin	Type	Description
XI	76	I	**Xtal In** Clock or crystal input connection 24.576 MHz (+/-100 ppm).
XO	77	O	**Xtal Out** 24.576 MHz crystal connection. If a clock is connected to XI, XO is disconnected.
RESET#	78	I	**Active Low Reset Input** This pin is connected to a 56K resistor to VDD and a 0.1 µF capacitor to ground yielding a power-on reset of approximately 3 ms.

2.2.4 Power to/from Bus Signals

Signal Name	Pin	Type	Description
PC[0:2]	23, 24, 25	I	**Power Class Indicator 0 (MSB) through 2 (LSB)** The PC[0:2] pins are strapped to indicate power consumed from or supplied to the bus (see P1394a specification, Table 8-3). At power-on the PC pins are read and the Pwr_class field (Address 04h[5:7]) is set. This value is transmitted in the pwr field of Self-ID packet zero.

Signal Definitions (Continued)

2.2.5 Power Supplies, Ground, Reserved, and No Connections

Signal Name	Pin	Type	Description
VDDIO	6, 34	PWR	**Digital Supply Connections** A split power plane with analog and digital power is recommended for the CS4103. A single delineation divides the analog and digital pins of the device. The power planes should be placed on either side of this delineation beneath corresponding analog and digital pins of the CS4103.
VSSIO	16, 28	GND	**Digital Ground Connections** A split ground plane with analog and digital grounds is recommended for the CS4103. A single delineation divides the analog and digital pins of the device. The ground planes should be placed on either side of this delineation beneath corresponding analog and digital pins of the CS4103.
VSS	21, 80	GND	**Digital Ground Connections** Connect this pin to the digital ground plane.
VDD	29, 79	PWR	**Digital Supply Connections** Connect this pin to the digital power plane.
VDDA	35, 54, 62, 63	PWR	**Analog Supply Connections** Connect this pin to the analog power plane.
GNDA	39, 40, 41, 64	GND	**Analog Ground Connections** Connect this pin to the analog ground plane.
R0	66	--	**Current Source Reference Resistor Connections**
R1	67	--	Sets the bias current for the CS4103 receivers. A resistor (5.76 KΩ +/–1%) is connected to R0 and R1. Place this resistor as close as possible to the CS4103.
VDDVCO	69	PWR	**VCO Analog Supply Connection** Connect this pin to the analog power plane.
GNDVCO	70	GND	**VCO Analog Ground Connection** Connect this pin to the analog ground plane.
VDDPLL	73	PWR	**PLL Analog Supply Connection** Connect this pin to the analog power plane.
GNDPLL	74	GND	**PLL Analog Ground Connection** Connect this pin to the analog ground plane.
RSVD0	32, 33	I	**Reserved** Tie these pins low.
RSVD1	31, 68	I	**Reserved** Tie these pins high.
NC	3, 9, 18, 20, 30, 36, 37, 38, 47, 48, 60, 65, 71, 72, 75	---	**No Connections (Total of 15)** These pins are not internally connected.

3.0 Register Descriptions

The CS4103 register set consists of Base registers and selectable Port/Page registers as illustrated in Figure 3-1. Addresses 00h through 07h access Base registers while addresses 08h through 0Fh access Port/Page registers. Port and Page information is selected using the Port_select and Page_select fields in the Base register at Address 07h. Of seven possible page addresses, three register pages are defined: the Port Status page (Page 0), Vendor Identification page (Page 1), and Vendor Specific page (Page 7). Port selection within a page is required for the Port Status Page. The Vendor Identification page has no per-port information and port selection has no effect on addressing this page. The Vendor Specific page may contain per-port registers but this implementation does not require port selection to access user defined registers.

Table 3-1 is a register map of the CS4103 showing the Base and Port/Page selection registers. The remaining sub-sections of this chapter provide details on register access and bit format information.

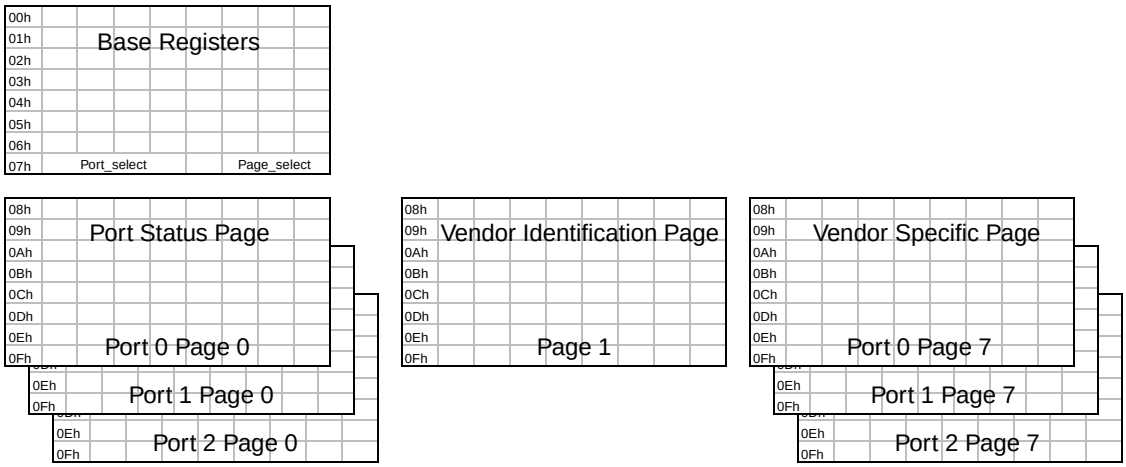


Figure 3-1. Base and Page/Port Registers

Table 3-1. Register Map

Address	0	1	2	3	4	5	6	7
00h	Physical_ID						R	PS
01h	RHB	IBR	Gap_count					
02h	Extended			RSVD	Total_ports			
03h	Max_speed			RSVD	Delay			
04h	Link_active	Contender	Jitter			Pwr_class		
05h	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
06h	RSVD							
07h	Page_select			RSVD	Port_select			
08h	Page[n], Port[n], Register-0							
09h	Page[n], Port[n], Register-1							
0Ah	Page[n], Port[n], Register-2							
0Bh	Page[n], Port[n], Register-3							
0Ch	Page[n], Port[n], Register-4							
0Dh	Page[n], Port[n], Register-5							
0Eh	Page[n], Port[n], Register-6							
0Fh	Page[n], Port[n], Register-7							

Register Descriptions (Continued)

3.1 REGISTER ACCESS

The register set of the CS4103 is accessed via the CS4210 OHCI device's PHYControl Register (BAR0+Offset ECh[11:0]). The PHYControl register, shown in Table 3-2, is used to read or write a CS4103 register.

To read a register, the address of the register is written to the regAddr field along with a 1 in the rdReg bit. When the read request has been sent to the CS4103 (through the LREQ pin), the rdReg bit is cleared to 0. When the CS4103 returns the register, the rdDone bit transitions to 1 and the IntEvent.phyRegRcvd interrupt (BAR0+Offset 80h[26]) is set. The address of the register received is placed in the rdAddr field and the contents in the rdData field. Software must not issue a read of CS4103 base register at Address 00h (see Table 3-5 on page 14). The most recently available contents of this register is reflected in the NodeID register (Table 3-3) of the CS4210.

To write to a CS4103 register, the address of the register is written to the regAddr field, the value to write to the wrData field, and a 1 to the wrReg bit. The wrReg bit is cleared when the write request has been transferred to the CS4103. Software must serialize all CS4103 register reads and writes. Only after the current CS4103 register read or write completes may software issue a different CS4103 register read or write.

For CS4210 register access information, refer to the CS4210 data sheet.

Table 3-2. CS4210 BAR0+Offset ECh: PHYControl Register

Bit	Name	Access	Reset	Description
31	rdDone	RU	Undef	**Read Done:** rdDone is cleared to 0 by the CS4210 when either rdReg or wrReg is set to 1. This bit is set to 1 when a register transfer is received from the CS4103.
30:28	RSVD	--	0	**Reserved**
27:24	rdAddr	RU	Undef	**Read Address:** This is the address of the register most recently received from the CS4103.
23:16	rdData	RU	Undef	**Read Data:** Contains the data read from the CS4103 register at rdAddr.
15	rdReg	RWU	0	**Read Register:** Set rdReg to initiate a read request to a CS4103 register. This bit is cleared when the read request has been sent. The wrReg bit must not be set while the rdReg bit is set.
14	wrReg	RWU	0	**Write Register:** Set wrReg to initiate a write request to a CS4103 register. This bit is cleared when the write request has been sent. The rdReg bit must not be set while the wrReg bit is set.
13:12	RSVD	--	0	**Reserved**
11:8	regAddr	RW	Undef	**Register Address:** regAddr is the address of the CS4103 register to be written or read.
7:0	wrData	RWU	Undef	**Write Data:** This is the contents to be written to a CS4103 register. Ignored for a read.

Table 3-3. CS4210 BAR0+Offset E8h: Node ID and Status Register

Bit	Name	Access	Reset	Description
31	iDValid	RU	0	**ID Valid:** This bit indicates whether or not the CS4210 has a valid node number. It is cleared when the bus reset state is detected and set again when the CS4210 receives a new node number from the CS4103. If iDValid is clear, software should not set ContextControl.run for either of the ATDMA contexts (request and response).
30	root	RU	0	**Root:** This bit is set during the bus reset process if the CS4103 is root.
29:28	RSVD	--	0	**Reserved**
27	CPS	RU	0	**Cable Power Status:** Set if the CS4103 is reporting that cable power status is OK (VP 8V).
26:16	RSVD	--	0	**Reserved**
15:6	busNumber	RWU	3FFh	**Bus Number**: This number is used to identify the specific 1394 bus this node belongs to when multiple 1394-compatible buses are connected via a bridge. This field is set to 3FFh on a bus reset.
5:0	nodeNumber	RU	Undef	**Node Number:** This number is the physical node number established by the CS4103 during self-identification. It is automatically set to the value received from the CS4103 after the self-identification phase. If the CS4103 sets the nodeNumber to 63, software should not set ContextControl.run for either of the ATDMA contexts (request and response).

Register Descriptions (Continued)

3.2 BASE REGISTER DESCRIPTIONS

Table 3-4 is a register map of the CS4103's Base registers. Table 3-5 provides the bit formats for these registers.

Table 3-4. Base Register Bit Map

Address	0	1	2	3	4	5	6	7
00h	Physical_ID						R	PS
01h	RHB	IBR	Gap_count					
02h	Extended			RSVD	Total_ports			
03h	Max_speed			RSVD	Delay			
04h	Link_active	Contender	Jitter			Pwr_class		
05h	Resume_int	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
06h	RSVD							
07h	Page_select			RSVD	Port_select			

Table 3-5. Base Registers

Bit	Name	Access	Reset	Description
Address 00h				
0:5	Physical_ID	R	Undef	**Physical ID:** The CS4103's node address determined during self-identification.
6	R	R	Undef	**Root:** Set when the node becomes root.
7	PS	R	Undef	**Cable Power Active:** This bit is set when cable power is detected above 7.5V. If cable power drops below 7.5V the PS bit will be cleared and the Pwr_fail bit set.
Address 01h				
0	RHB	RW	0	**Root Hold-off Bit:** When set, the CS4103 will attempt to become root during the next tree identify process which is subsequent to a bus reset.
1	IBR	RW	0	**Initiate Bus Reset:** When set, a non-arbitrated long bus reset of 167 µs will be issued by the CS4103. This bit is self clearing.
2:7	Gap_count	RW	3Fh	**Gap Count:** Arbitration gap times are tuned to minimize bus idle time with this field. Gap times may be optimized for a specific bus configuration. Two bus resets return gap_count to 3Fh.
Address 02h				
0:2	Extended	R	111	**Extended:** A value of seven is assigned to this field indicating that the extended PHY register map has been implemented.
3	RSVD	--	--	**Reserved**
4:7	Total_ports	R	1100	**Total Ports:** This field shows the number of ports implemented by the CS4103. The CS4103 utilizes three ports.
Address 03h				
0:2	Max_speed	R	010	**Maximum Speed:** Indicates CS4103 operational speeds. A value of 010 indicates the CS4103 supports 98.304, 196.608, and 393.216Mbit/sec operation.
3	RSVD	--	--	**Reserved**
4:7	Delay	R	0000	**Delay:** Worst-case repeater delay equals 144 + (delay * 20) ns.

Register Descriptions (Continued)

Table 3-5. Base Registers (Continued)

Bit	Name	Access	Reset	Description
Address 04h				
0	Link_active	R/W	1	**Link Active:** The logical AND of Link_active and LPS active sets the L bit of the nodes self-ID packet.
1	Contender	R/W	0	**Contender:** Cleared or set by software to control the value of the C (Contender) bit transmitted in self-ID packet zero.
2:4	Jitter	R	000	**Jitter:** The difference between the fastest and slowest repeater delay, expressed as (jitter + 1) * 20ns.
5:7	Pwr_class	R/W	*	**Power Class:** Controls the value of the pwr field transmitted in the self_ID packet. Upon reset, the value of the PC[0:2] strapping pins is loaded into this field. This field may be subsequently written by software. Power Class is application dependent (see P1394a specification, Table 8-3). *Reset value is application dependent.
Address 05h				
0	Resume_int	RW	0	**Resume Interrupt Enable:** When set to one, the CS4103 sets Port_event to one if resume operations commence for any port.
1	ISBR	RW	0	**Initiate short (arbitrated) Bus Reset:** When set, an arbitrated short bus reset will be issued by the CS4103. This bit is self-clearing.
2	Loop	RW	0	**Loop Detect:** Indicates a loop in the cable topology. A write of one to this bit clears it to zero. A software clear of this bit will occur if a cable loop is present.
3	Pwr_fail	RW	0	**Cable Power Failure Detect:** Set to one when the PS bit changes from one to zero. A write of one to this bit clears it to zero.
4	Timeout	RW	0	**Arbitration State Machine Timeout:** A write of one to this bit clears it to zero.
5	Port_event	RW	0	**Port Event Detect:** The CS4103 sets this bit to one if any of Connected, Bias, Disabled or Fault change for a port whose Int_Enable bit is one. The CS4103 also sets this bit to one if resume operations commence for any port and Resume_int is one. A write of one to this bit clears it to zero.
6	Enab_accel	RW	0	**Enable Arbitration Acceleration:** When set, the CS4103 uses the enhancements specified in clause 7.10. CS4103 behavior is unspecified if the value of Enab_accel is changed while a bus request is pending.
7	Enab_multi	RW	0	**Enable Multi-speed Packet Concatenation:** When set, the link signals the speed of all packets to the CS4103.
Address 06h				
0:7	RSVD	--	--	**Reserved**
Address 07h				
0:2	Page_select	RW	000	**Page Select:** Selects one of eight register pages of which only pages 0, 1, and 7 are defined. The selected page is accessible at Addresses 08h through 0Fh.
3	RSVD	--	--	**Reserved**
4:7	Port_select	RW	0000	**Port Select:** Selects per port information of a register page. If a register page has per port registers this field selects which port registers are accessible at Addresses 08h through 0Fh.

Register Descriptions (Continued)

3.3 PORT STATUS: PAGE 0, PORTS[0:2]

The Port Status page is accessed by setting the Page_select field to 000b in the Base register at Address 07h. Status information is selected per-port within the Port Status page by setting the Port_select field in the Base register at Address 07h. Three sets of port status registers, one per-port, are indexed by the Port_select field. Valid Port_select values are 000b, 001b, and 010b.

Table 3-6. Port Status: Page 0 Bit Map

Address	0	1	2	3	4	5	6	7
08h	AStat		BStat		Child	Connected	Bias	Disabled
09h	Negotiated_speed			Int_Enable	Fault	RSVD		
0Ah-0Fh	RSVD							

Table 3-7. Port Status: Page 0 Registers

Bit	Name	Access	Reset	Description
Address 08h			**Page 0, Port[n], Register-0**	
0:1	AStat	R	Undef	**TPA Status:** TPA differential line state detected by the TPA arbitration comparators of the port specified by Port_select. 00 = Invalid 01 = 1 10 = 0 11 = Z
2:3	BStat	R	Undef	**TPB Status**: TPB differential line state detected by the TPB arbitration comparators of the port specified by Port_select. 00 = Invalid 01 = 1 10 = 0 11 = Z
4	Child	R	Undef	**Child:** When set, the port specified by Port_select is a child. If clear, the port is a parent.
5	Connected	R	0	**Connected:** When set, the port specified by Port_select is connected.
6	Bias	R	Undef	**Bias:** When set, the port specified by Port_select detects TPBias from a connected PHY.
7	Disabled	RW	0	**Disable:** When set, the port specified by Port_select is disabled.
Address 09h			**Page 0, Port[n], Register-1**	
0:2	Negotiated_ speed	R	Undef	**Negotiated Speed:** The maximum negotiated speed between the port specified by Port_select and a connected port. 000 = 100 Mbits/sec 001 = 200 Mbits/sec 010 = 400 Mbits/sec All other settings are reserved.
3	Int_Enable	RW	0	**Interrupt Enable:** When set, the port specified by Port_select, port event interrupts are enabled. A change in connected, bias, disabled, or fault states will set the Port_event bit.
4	Fault	RW	0	**Fault:** A Suspend or Resume operation error of the port specified by Port_select will set this bit. Writing a one to the bit will clear it to zero.
5:7	RSVD	--	--	**Reserved**
Address 0Bh-0Fh			**Page 0, Port[n], Register-2 through Register-7**	
0:7	RSVD	RW	00h	**Reserved:** Do not set bits in these fields. Setting bits in these fields may cause noncompliant or unspecified behavior.

Register Descriptions (Continued)

3.4 VENDOR IDENTIFICATION: PAGE 1

All registers of the Vendor Identification page are accessible by setting the Page_select field to 001b in the Base register at Address 07h. The Vendor Identification page has no per-port registers. The value of Port_select is ignored when addressing this page.

Table 3-8. Vendor ID: Page 1 Bit Map

Address	0	1	2	3	4	5	6	7
08h	Compliance_level							
09h	RSVD							
0Ah	Vendor_ID[23:16] (MSB)							
0Bh	Vendor_ID[15:8]							
0Ch	Vendor_ID[7:0] (LSB)							
0Dh	Product_ID[23:16] (MSB)							
0Eh	Product_ID[15:8]							
0Fh	Product_ID[7:0] (LSB)							

Table 3-9. Vendor ID: Page 1 Registers

Bit	Name	Access	Reset	Description
Address 08h				**Page 1, Register-0**
0:7	Compliance_ level	R	01h	**Standard Compliance Indicator:** A value of 01h indicates that the CS4103 complies to the IEEE P1394a standard. 01h = IEEE P1394a compliant All other values are not specified.
Address 09h				**Page 1, Register-1**
0:7	RSVD	--	--	**Reserved**
Address 0Ah				**Page 1, Register-2**
0:7	Vendor_ID[23:16]	R	08h	**Vendor ID:** The MSB of a 24-bit value identifying National Semiconductor as the vendor. Works in conjunction with Addresses 0Bh and 0Ch.
Address 0Bh				**Page 1, Register-3**
0:7	Vendor_ID[15:8]	R	00h	**Vendor ID:** A 24-bit value identifying National Semiconductor as the vendor. Works in conjunction with Addresses 0Ah and 0Ch
Address 0Ch				**Page 1, Register-4**
0:7	Vendor_ID[7:0]	R	17h	**Vendor ID:** The LSB of a 24-bit value identifying National Semiconductor as the vendor. Works in conjunction with Addresses 0Ah and 0Bh.
Address 0Dh				**Page 1, Register-5**
0:7	Product_ID	R	00h	**Product ID**: The MSB of a 24-bit value identifying the device as the CS4103. Works in conjunction with Addresses 0Eh and 0Fh.
Address 0Eh				**Page 1, Register-6**
0:7	Product_ID	R	00h	**Product ID:** A 24-bit value identifying the device as the CS4103. Works in conjunction with Addresses 0Dh and 0Fh.
Address 0Fh				**Page 1, Register-7**
0:7	Product_ID	R	02h	**Product ID:** The LSB of a 24-bit value identifying the device as the CS4103. Works in conjunction with Addresses 0Dh and 0Fh.

Register Descriptions (Continued)

3.5 VENDOR SPECIFIC: PAGE 7, PORTS[0:2]

The Vendor Specific page is reserved for vendor use. It may contain per-port registers but this implementation does not require port selection to access user defined registers. The Vendor Specific page is accessible by setting the Page_select field in the Base register at Address 07h to 0111b.

Table 3-10. Vendor Specific: Page 7 Bit Map

Address	0	1	2	3	4	5	6	7
08h-0Eh	RSVD							
0Fh	RSVD			PD[0]	PD[1]	RSVD		

Table 3-11. Vendor Specific: Page 7 Registers

Bits	Name	Access	Reset	Description
Addresses 08h-0Eh		**Page 7, Port[n], Register-0 through Register-6**		
0:7	RSVD	RW	00h	**Reserved:** Do not set bits in these fields. Setting bits in these fields may cause noncompliant or unspecified behavior.
Addresses 0Fh		**Page 7, Port[n], Register-7**		
0:2	RSVD	RW	00h	**Reserved:** Do not set bits in these fields. Setting bits in these fields may cause noncompliant or unspecified behavior.
3:4	PD[1:0]	RW	00	**Power Down Mode:** The CS4103 will transition to a low power state defined by these bits when the PHY-Link interface is disabled and the PHY ports are in the disabled, disconnected or suspended state. 00 = No Power Down. 01 = Stop PLL and 50 MHz clock. 10 = Stop 50 MHz clock. 11 = Stop Crystal, PLL, and 50 MHz clock.
5:7	RSVD	RW	00h	**Reserved:** Do not set bits in these fields. Setting bits in these fields may cause noncompliant or unspecified behavior.

4.0 Electrical Characteristics

This section provides information on absolute maximum ratings, recommended operating conditions, and DC/AC characteristics for the Geode CS4103.

4.1 ABSOLUTE MAXIMUM RATINGS

Table 4-1 lists the absolute maximum ratings for the CS4103. Stresses beyond the listed ratings may cause permanent damage to the device. Exposure to conditions beyond these limits may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also reduce useful life and reliability. These are stress ratings only and do not imply that operation under any conditions other than those listed in Table 4-1 is possible.

4.2 OPERATING CONDITIONS

Table 4-2 lists the operating conditions for the CS4103.

Table 4-1. Absolute Maximum Ratings

Parameter	Units
Supply Voltage, V_{DD}	–0.5V to 4.1V
Input Voltage	–0.5V to V_{DD}+0.5V
Output Voltage	–0.5V to V_{DD}+0.5V
Storage Temperature, T_{STG}	–65°C to 150°C
ESD Tolerance	2000V
Lead Temperature, T_L	230°C (Soldering 10 seconds)

Table 4-2. Operating Conditions

Parameter	Units
Supply Voltage, V_{DD}	3.0V to 3.6V
Operating Temperature, T_A	0°C to 70°C
Crystal	24.576 MHz +/–100 ppm

Electrical Characteristics (Continued)

4.3 DC SPECIFICATIONS

Table 4-3. IEEE-P1394A PHY-Link Interface

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DD}	Supply Voltage	3.0		3.6	V	
I_{DD}	Supply Current		120		mA	
I_{SB}	Standby Supply Current:					
	PD Mode 0: Page 7, Address 0Fh[4:3] = 00		42		mA	PHY-Link interface inactive
	PD Mode 1: Page 7, Address 0Fh[4:3] = 01		15		mA	
	PD Mode 2: Page 7, Address 0Fh[4:3] = 10		6.5		mA	
	PD Mode 3: Page 7, Address 0Fh[4:3] = 11		5		mA	
V_{OH}	Output High Voltage (undifferentiated)	2.8			V	I_{OH} = –4mA
V_{OL}	Output Low Voltage (undifferentiated)			0.4	V	I_{OL} = 4mA
V_{OHD}	Output High Voltage (differentiated)	V_{DD}–0.4			V	I_{OH} = –9mA @ V_{DD} = 3.0V
V_{OLD}	Output Low Voltage (differentiated)			0.4	V	I_{OL} = 9mA @ V_{DD} = 3.0V
V_{IH}	Input High Voltage (undifferentiated), DATA[0:7], CTRL[0:1], LREQ, LPS, PC[0:2], DIRECT	2.6		V_{DD}+10%	V	V_{DD} = 3.3V
V_{IL}	Input Low Voltage (undifferentiated), DATA[0:7], CTRL[0:1], LREQ, LPS, PC[0:2], DIRECT			0.7	V	
V_{LIT+}	Input Rising Threshold, LPS			V_{LREF}+1	V	V_{LREF} = 1.0V
$V_{LIT–}$	Input Falling Threshold, LPS	V_{LREF}+0.2			V	V_{LREF} = 1.0V
V_{IT+}	Hysteresis input rising threshold (differentiated) DATA[0:7], CTRL[0:1], LREQ	V_{REF}+0.3		V_{REF}+0.8	V	
$V_{IT–}$	Hysteresis input falling threshold (differentiated), DATA[0:7], CTRL[0:1], LREQ	V_{REF}–0.8		V_{REF}–0.3	V	
V_{LREF}	Reference Voltage		1.0		V	
I_{IH}	Input High Leakage Current			10	µA	
I_{IL}	Input Low Leakage Current			10	µA	
C_{IN}	Input Pin Capacitance			4	pF	

Electrical Characteristics (Continued)

4.4 AC SPECIFICATIONS

Table 4-4. IEEE-1394A PHY-Link Interface Timings

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
	SCLK Frequency	49.152MHz +/-100ppm			MHz	
	SCLK Duty Cycle	45		55	%	
t_{PD1}	Delay Time, SCLK High to Initial Instance of DATA[0:7] and CTRL[0:1] Valid	0.5		13.5	ns	
t_{PD2}	Delay Time, SCLK High to Subsequent Instances of DATA[0:7] and CTRL[0:1] Valid	0.5		13.5	ns	
t_{PD3}	Delay Time, SCLK High to DATA[0:7] and CTRL[0:1] Invalid	0.5		13.5	ns	
t_{PSU}	Setup Time, DATA[0:7], CTRL[0:1], and LREQ before SCLK High	6			ns	
t_{PH}	Hold Time, DATA[0:7], CTRL[0:1], and LREQ after SCLK High	0			ns	
t_R	Rise Time, DATA[0:7], CTRL[0:1], and SCLK	0.7		2.4	ns	
t_F	Fall Time, DATA[0:7], CTRL[0:1], and SCLK	0.7		2.4	ns	

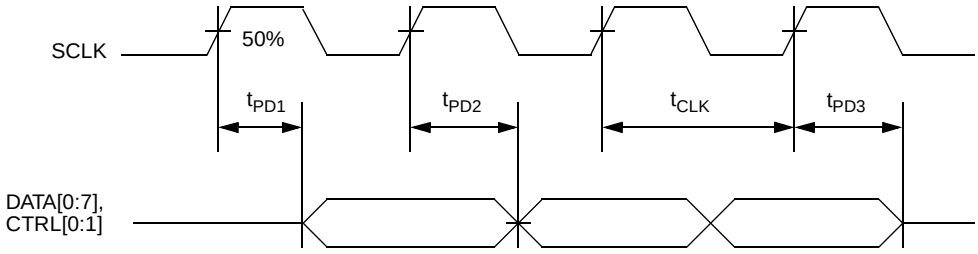


Figure 4-1. SCLK to Data Valid Timing Waveform

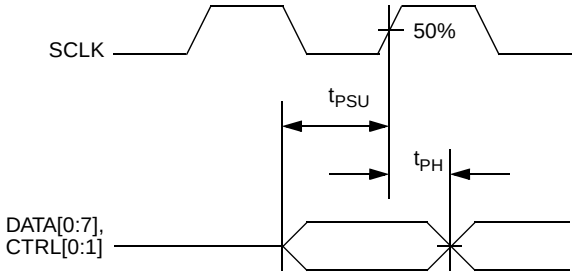


Figure 4-2. Setup and Hold Timing Waveform

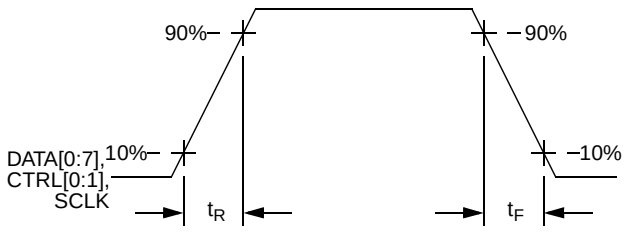


Figure 4-3. Rise and Fall Timing Waveforms

Electrical Characteristics (Continued)

Table 4-5. IEEE 1394 Cable Interface Timings

Symbol	Parameter	Min	Max	Unit	Conditions
I_{S100}	Common Mode Signaling at 100 Mbit/sec	–0.81	0.44	mA	
I_{S200}	Common Mode Signaling at 200 Mbit/sec	–4.84	–2.53	mA	
I_{S400}	Common Mode Signaling at 400 Mbit/sec	–12.40	–8.10	mA	
V_{ICM}	Common Mode Input Voltage TPB+, TPB–				
	100 Mbit/sec	1.165	2.515	V	
	200 Mbit/sec	0.935	2.515	V	
	400 Mbit/sec	0.523	2.515	V	
V_{OCM}	Common Mode output Voltage TPA+, TPA–	1.665	2.015	V	
V_{OD}	Differential Output Voltage	172	265	mV	
I_{OD}	Differential Output Current	–1.05	1.05	mA	
V_{ID}	Differential Input Voltage	118	265	mV	
V_{AP}	Positive Arbitration Threshold	89	168	mV	
V_{AN}	Negative Arbitration Threshold	-168	–89	mV	
V_{S200}	S200 Speed Signal Voltage	45	139	mV	
V_{S400}	S400 Speed Signal Voltage	266	445	mV	
I_{OB}	TPBias Output Current	–3	3	mA	
T_{OR}	Transmit Output Rise Time	0.5	1.2	ns	
T_{OF}	Transmit Output Fall Time	0.5	1.2	ns	
	Transmitter Skew		0.10	ns	
	Transmitter Jitter		0.15	ns	
	Receive Input Jitter				
	100 Mbit/sec		1.08	ns	
	200 Mbit/sec		0.50	ns	
	400 Mbit/sec		0.315	ns	
	Receive Input Skew				
	100 Mbit/sec		0.80	ns	
	200 Mbit/sec		0.55	ns	
	400 Mbit/sec		0.50	ns	

Electrical Characteristics (Continued)

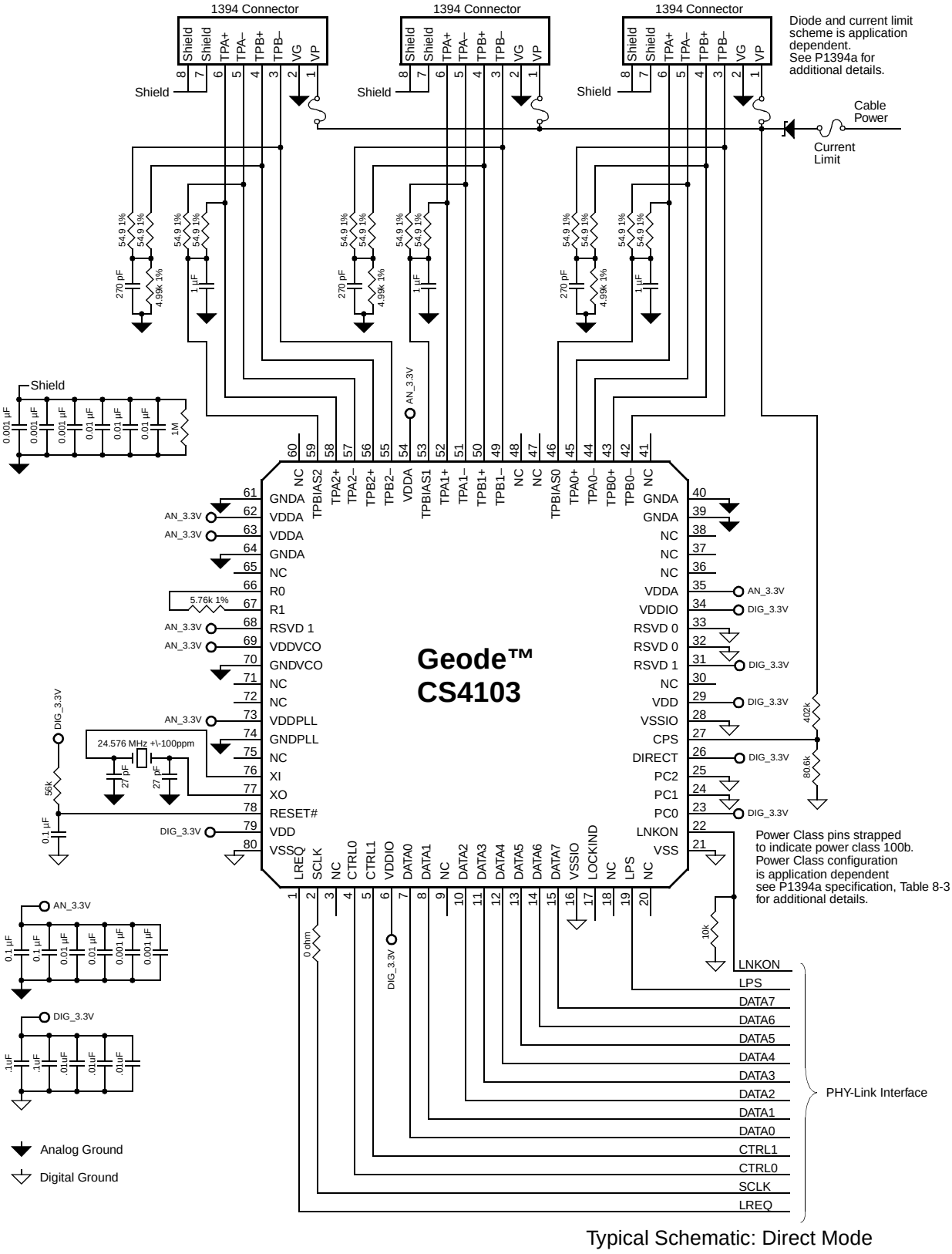
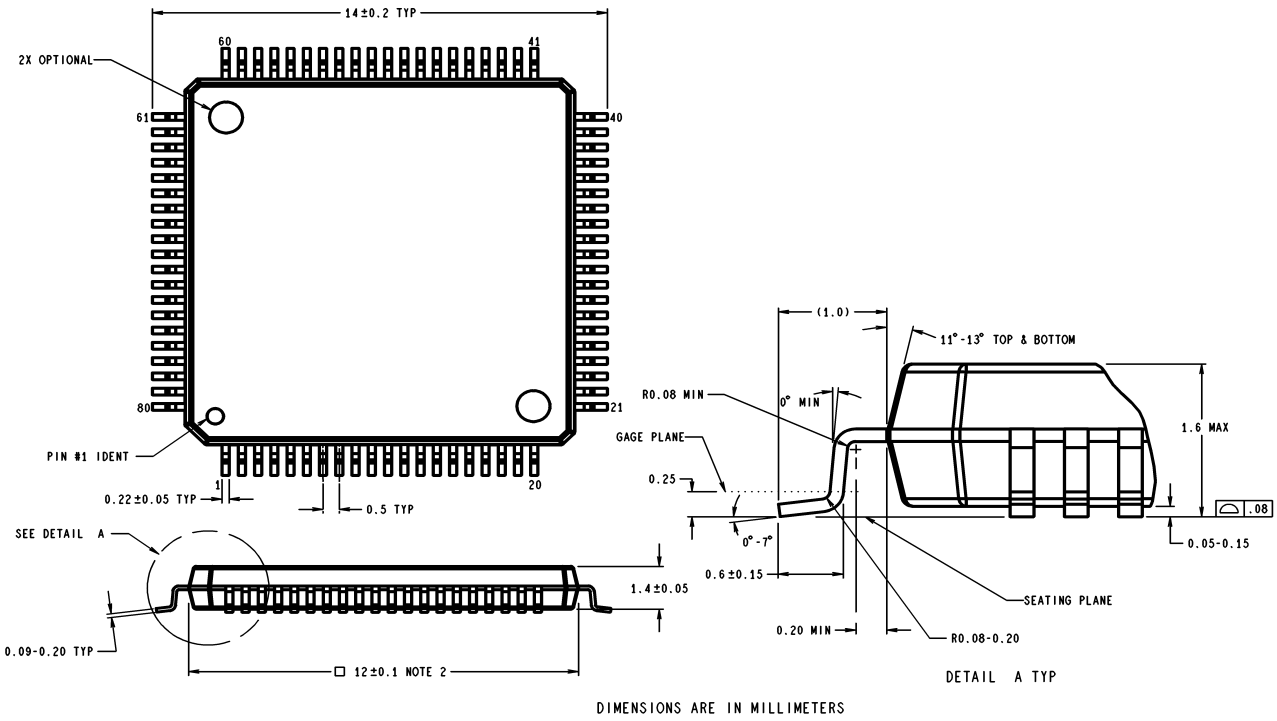


Figure 4-4. Typical Application

5.0 Physcial Dimensions



VHG80A (Rev C)

Note: 1 Standard lead finish: 7.62 micrometers minimum plating (8/15) thickness on copper.

2 Dimension does not include mold protrusion. Maximum allowable mold protrusion 0.25 mm per side.

3. Reference JEDEC registration MS-026, variation BDD, dated February 1999.

Figure 5-1. 80-Pin Low-Profile Quad Flat Pack (LQFP)
Order Number: CS4103VHG

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Email: nsj.crc@jksmtp.nsc.com